#3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Khan, et al.
Serial No. 09/886,741
Filing Date: June 21, 2001

Examiner: Unknown
Art Group: Unknown
Our file no. 00100.01.0068
Docket No. 0100680

Title: **MULTI-DIE MODULE AND METHOD THEREOF**

Assistant Commissioner for Patents
Attn: Group Director, Technology Center 2800
U.S. Patent and Trademark Office
Washington, D.C. 20231

Certificate of First Class Mailing
I hereby certify that this paper is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Assistant Comm. for Patents, Attn: Group Director, Technologiy Center 2800, U.S. Patent & Trademark Office, Washington, D.C. 20231, on this date.
2-13-02 Karenina Oliver
Date *Karenina Oliver*

PETITION TO MAKE SPECIAL FOR NEW APPLICATION UNDER MPEP §708.02

Sir:

Applicant hereby Petitions to make this new application, which has not received any examination by the Examiner, special under MPEP §708.02 (VIII).

1. All claims in this case are directed to a single invention. If the Office determines that all the claims presented are not obviously directed to a single invention, then Applicant will make an election without traverse as a prerequisite to the grant of special status.

2. A pre-examination search has been made by a professional searcher in the following field(s) of search: class(es) 257; 438; sub-class(es) 678 and 723; 106 and 107.

3. There is submitted herewith a copy of the references deemed the most closely related to the subject matter encompassed by the pending claims. In addition, form PTO-1449 is also enclosed.

4. There is submitted herewith a detailed discussion of the references, pursuant to MPEP §708.02(VIII) for those references most closely related to the subject matter encompassed by the claims.

Please charge any fees required under 37 C.F.R. §1.17(i) ($130.00) to Deposit Account No. 50-0441. The Commissioner is hereby authorized to charge any additional fees which may

required by this paper or credit any overpayment in the instant matter to Deposit Account No. 50-0441.

A duplicate of this paper is attached.

Respectfully submitted,

By _____
Loren H. McRoss
Registration No. 40,427

Date: February 13, 2002

VEDDER, PRICE, KAUFMAN &
KAMMHOLZ
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7500
FAX: (312) 609-5005

PETITION TO MAKE SPECIAL FOR NEW APPLICATION UNDER MPEP §708.02

DETAILED DISCUSSION OF MOST CLOSELY RELATED REFERENCES

1. Discussion of the Mess reference (U.S. Patent No. 6,335,221)

Mess is directed to a molding machine for providing one-side encapsulation of electronic devices. As is disclosed, for example, at col. 5, lines 19-34, the resulting device includes one or more semiconductor chips which are encapsulated by injecting a melted plastic into a mold which encloses the semiconductor chips. However, the resulting device does not have a structure including a packaged semiconductor die mounted on the same substrate surface as the encapsulated die as defined in the pending claims. In addition, Mess does not disclose that the encapsulated die is an "...unpackaged semiconductor die..." as defined in the pending claims. Moreover, a method for fabricating a multi-die module including an encapsulated, unpackaged die and at least one packaged semiconductor die is also not disclosed in Mess. Accordingly, the presently claimed invention is allowable over Mess.

2. Discussion of the Dudderar, et al. reference (U.S. Patent No. 6297,551)

Dudderar, et al. is directed to a circuit package exhibiting improved EMI characteristics and method of making the same. The improved EMI characteristics are provided by an EMI shield being placed about the resulting circuit elements which are maintained in a flip-chip configuration (*see*, for example, col. 2, lines 50-52 and col. 2, line 63-col. 3, line 8). This reference does not disclose or suggest fabricating a multi-die module having the structured as defined in the pending claims. Moreover, Dudderar, et al. and the present invention are directed to different problems. More specifically, Dudderar, et al. is directed to negating the effects of EMI; whereas, the presently claimed invention is directed to a multi-die circuit structure exhibiting improved manufacturing and testing characteristics. Accordingly, the Applicants submit that the presently claimed invention is allowable over Dudderar, et al.

3. Discussion of the Bertin, et al. reference (U.S. Patent No. 5,807,791)

Bertin, et al. is directed to a multi-chip structure where redundant elements (e.g. I/O ports) are maintained in a separate chip which is oriented in a stacked relationship with respect to the non-redundant (e.g. non-I/O) chips that comprise a circuit structure. Although Bertin, et al. is

directed to a multi-chip semiconductor structure, the disclosed structure does not anticipate, nor teach or suggested the presently claimed structure or method of fabricating the same. For example, Bertin, et al. does not disclose a multi-die structure including:

> "...an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure having a rectangular footprint; and
> a packaged semiconductor die mounted on the first surface of the substrate..."

as defined in the pending claims. In fact, Bertin, et al. does not disclose the use of unpackaged die at all. Moreover, the method of fabricating a multi-die module incorporating unpackaged and packaged die in the same circuit structure is also neither disclosed nor suggested in Bertin, et al. Accordingly, the present claims are allowable over Bertin, et al.

4. Discussion of the Sasov reference (U.S. Patent No. 5,986,886)

Sasov is directed to an electronic module where the underlying components are interconnected in a side-by-side fashion to a corrugated commutation board (*see*, col. 4, lines 13-16 and FIG. 3). The commutation board, through its corrugated properties is flexible and mallable. Therefore, the resulting module can be used in various configurations – from compressed fashion (*see*, col. 4, lines 33-37) to an extended fashion (*see*, col. 4, lines 45-51). However, as the electronic components are not located on the same substrate (*see*, FIG. 3 and col. 4, lines 33-37), the disclosed structure neither discloses or suggests the claimed multi-die structure of the present invention. Moreover, there is no discussion of encapsulating, in a rectangular footprint, and unpackaged die or corresponding method for producing the same. Consequently, the presently claimed invention is allowable over Sasov.

5. Discussion of the Collander reference (U.S. Patent No. 5,872,700)

Collander is directed to interconnecting the components of an integrated circuit structure with an insulating tape where the tape has contact pads and conduction trace(s) formed therein (*see*, FIG. 13 and col. 5, lines 52-66). Although the disclosed interconnection method is described with reference to a multi-component structure (*see*, for example, col. 3, line 66-col. 4, line 17), the structure does not include the combination of unpackaged and packaged being mounted on the same substrate surface as defend in the pending claims.

Additionally, as Collander is silent on the structural aspects of the underlying circuit thereof, such reference also does not anticipate or render obvious the claimed method of producing such claimed structure. Consequently, the presently claimed invention is allowable over Collander.